

CLASS-BASED NEURAL NETWORK METHOD FOR FAULT LOCATION OF LARGE-SCALE ANALOGUE CIRCUITS

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ABSTRACT

A new method for fault diagnosis of large-scale analogue circuits based on the class concept is developed in this paper. A large analogue circuit is decomposed into blocks/sub-circuits and the nodes between the blocks are classified into three classes. Only those sub-circuits related to the faulty class need to be treated. Node classification reduces the scope of search for faults, thus reduced after-test time. The proposed method is more suitable for real-time testing and can deal with both hard and soft faults. Tolerance effects are taken into account in the method. The class-based fault diagnosis principle and neural network based method are described in some details. Two non-trivial circuit examples are presented, showing that the proposed method is feasible.

1. INTRODUCTION

Fault diagnosis and testing of analogue circuits has become an active research area since 1970's [1, 2]. Various useful techniques have been proposed in the literature such as the fault dictionary technique, parameter identification technique, and fault verification method [1-13]. Analogue circuit fault diagnosis remains extremely difficult and becomes the bottleneck of automatic testing of mixed-signal circuits. This is because of the difficulty of measuring currents, the lack of good fault models similar to stuck-at-one and stuck-at-zero fault models in digital circuit test, the tolerance of components and the nonlinear nature of the analog circuits (the relationship between the circuit responses and the component characteristics is nonlinear, even if the circuit is linear). Therefore, only the fault dictionary technique is widely appreciated in practical engineering application among the various techniques in the literature because of its simplicity and the effectiveness. However, the traditional fault dictionary technique is based on the Neumann computer principle. It has its own vital weakness, that is, it can only detect hard faults and cannot cope with soft faults. Also, its application is largely limited to small to medium analogue circuits. Furthermore, it cannot diagnose faults in real-time for large-scale circuits.

In order to solve the above problems of the traditional fault dictionary method, several artificial neural network based approaches have been proposed for analogue fault diagnosis and they have proved very promising [6-13]. The neural network-based fault dictionary technique [12, 13] can overcome the weakness of the traditional

Neumann computer-based dictionary. It can locate and identify not only hard faults but also soft faults. Furthermore, in the neural network based fault dictionary technique, looking up a dictionary to locate and identify faults is actually carried out at the same time of setting up the dictionary. It thus reduces the computation and has a better real-time feature. However, not much work has been done on the fault diagnosis of large-scale analog circuits using artificial neural networks. In a recently proposed method for fault diagnosis of large-scale circuits with tolerance [13], the large-scale circuits are decomposed to several sub-circuits and a back propagation neural network (BPNN) is applied for fault location in each sub-circuit. The method can diagnose not only catastrophic faults but also parametric ones.

In order to further lessen the complexity of after-test diagnosis, a neural network approach based on the class concept [3-5] is presented in this paper. A set of some components of the same characteristic in a system is called a *class*. A system may be divided into several classes. The characteristics of all the components in each class are the same. Thus if we can determine the characteristic of any component in a class, all the other components in the class can be determined. From the fault diagnosis viewpoint, the class is fault free if a component in the class is fault free. In this paper, the nodes are classified. The main rule is that: two nodes belong to the same class if their characteristics are the same. According to this rule, the nodes in a circuit can be divided into different classes. We only need to diagnosis the most possible faulty sub-circuits whose nodes belong to the faulty classes, and thus the search space for fault diagnosis is largely reduced. The class method is suitable for any scale of circuits in principle, we particularly develop a procedure for block-based large-scale circuits with classification of tearing nodes. For the final component-level fault diagnosis within sub-circuits/blocks, the BPNN-based fault dictionary technique is used, which, together with the computation-less node classification concept and circuit decomposition method, make it possible to identify the faults of large-scale analogue circuits in real-time.

2. FAULT DIAGNOSIS BASED ON CLASS CONCEPT

Without a loss of generality, it is assumed that the circuit under consideration has $m+1$ accessible nodes among total n nodes, and the $(m+1)^{\text{th}}$ node is taken as a reference, and the set of the accessible nodes is $[n_1, n_2, \dots, n_m]$. The actual accessible node voltage vector is $V=[V_1, V_2, \dots, V_m]^T$, and the nominal voltage vector is $V_0=[V_{10},$

$V_{20}, \dots, V_{m0}]^T$ when all components in the circuit have their nominal values.

We assume that for any accessible node, its node-voltage sensitivity with respect to any component is not zero. We also take the fact into account that the effects of two independent analog faults are highly unlikely to cancel at the test nodes. It is obvious that

Theorem 1: The necessary and almost sufficient condition for a system without tolerance to be fault free is the test vector V is equal to the nominal V_0 when the same stimulus is applied to the actual and nominal circuits.

The node voltage of the i^{th} node will become an interval when the circuit is with tolerance. Let the nominal interval be $[V_{i01}, V_{i02}]$, which can be calculated before test by the Monte Carlo method, nonlinear programming method, or interval algebra algorithm. The nominal interval vector V_0 can be thus obtained.

Theorem 2: The necessary and almost sufficient condition for a system with tolerance to be fault free is that the test vector V is within the nominal voltage interval V_0 when the same stimulus is applied to the actual and nominal circuits.

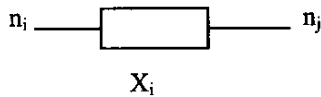


Fig.1. A typical branch and related nodes

Consider Figure 1 where a component X_i is between nodes n_i and n_j . Component X_i is called the *relevant component* of nodes n_i and n_j , and nodes n_i and n_j are called the *neighbor nodes*. There are three possibilities: (1) the voltages of nodes n_i and n_j are all normal; (2) one of them is normal and the other is abnormal; (3) the voltages of nodes n_i and n_j are all abnormal. The accessible nodes in a system can be accordingly classified into three classes:

Class 1: is the set of the nodes whose voltages are normal (fall within their intervals).

Class 2: contains the nodes whose voltages are abnormal (fall outside their intervals) and at most one of the node voltages among its neighbor nodes (not including the reference node) is abnormal.

Class 3: consists of the nodes that satisfy one of the following:

- The node voltages are abnormal, and at least two of the node voltages among its neighbor nodes (not including the reference node) are abnormal.
- The node voltages are abnormal and only one of the node voltages among its neighbor nodes is abnormal, but the reference node is one of its neighbor nodes.

It is obvious that the relevant branches or components in Class 1 are fault free because their node voltages are normal, while the ones in Class 2 and Class 3 are "suspicious" components. And the components in Class 3

are more likely to be faulty than those in Class 2.

Theorem 3: The only possible faulty components in Class 2 are those in the common branches of Class 2 and Class 3.

Proof: Without loss of generality, it is assumed that node "a" is one of the nodes in Class 2 of the circuit and it is linked to its k neighbor accessible nodes (1,2,3... k), see Figure 2, whose node voltages are V_1, V_2, \dots, V_k . By definition there is only one of V_1, V_2, \dots, V_k beyond its normal scope of Class 2; let it be V_1 . Thus nodes 2, 3, ... k are in Class 1, and node 1 is a node in either Class 2 or Class 3.

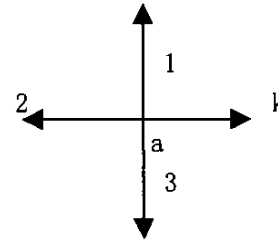


Fig. 2. A node "a" in Class 2

Note that the reference node is not in the k nodes. Supposing that one of the branches 2-a, 3-a, ..., k-a be faulty, the nodes voltages of nodes 2, 3, ... k will all be beyond their normal scopes. This is in contrary to the assumption that node a is in Class 2. Thus only branch 1-a can be faulty. Node 1 must be in Class 3. If node 1 is in Class 2, then the branch 1-a will be an inner branch of Class 2. The fault in branch 1-a will thus only affect the node voltages of V_1 and V_a , and have no effect on the other node voltages of V_1, V_2, \dots, V_k . That is, the sensitivity of any node voltage except V_1 and V_a with respect to the component in branch 1-a is zero. This is in conflict with our assumption. [End of proof]

Since the faulty components are in Class 3, including the common branches of Class 2 and Class 3, so the scale of the diagnosis problem is quickly reduced to Class 3. The remaining task is simply to find the fault components in Class 3, equivalently the sub-circuits/blocks related to Class 3. This can be done using the neural network method. For a single fault diagnosis of a linear circuit, the following expression containing the accessible node

$$\text{voltage increments } \Delta V_i / (\sum_{j=1}^m \Delta V_j^2)^{1/2} \quad (i=1,2 \dots m)$$

is a constant whether the fault is a soft or hard one. It depends only on the circuit topology and its nominal

parameter values. Thus $\Delta V_i / (\sum_{j=1}^m \Delta V_j^2)^{1/2}$ can be

extracted as the feature vectors for the fault dictionary, passing through the BPNN (back-propagation neural network). The BPNN will not be trained ready until it converges at the target value.

After test, the measured feature vector is applied to the trained BPNN, and the output of the BPNN is the order of the faults. The steps involved in the diagnosis process

3. FAULT LOCATION OF LARGE-SCALE CIRCUITS

For large-scale circuit diagnosis, a block-based methodology should be used for various practical reasons. In the proposed method, a large-scale analogue circuit is first partitioned into several sub-networks meeting the following requirements:

- The incident nodes between the sub-networks must be accessible.
- Ensure that the sub-networks are uniquely diagnosable.
- The sub-networks must be mutually uncoupled both in topology and in parameters.
- The networks must be the minimum-scale networks, that is, it cannot be torn to smaller sub-networks

Then the classification of accessible nodes is carried out. From the discussion in the above we know that the sub-circuits containing only Class 1 and Class 2 are fault free. So we only need to identify the faults in the sub-networks containing Class 3 nodes. Thus the diagnosis procedure can be simplified as follows:

- ①. Divide the large-scale circuit into sub-circuit 1, sub-circuit 2, ... and sub-circuit n

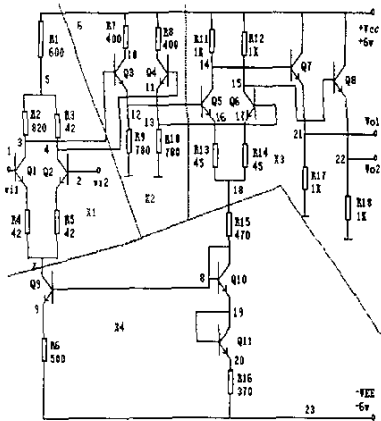


Fig.3. A voltage amplifier circuit

- ②. Define the faults of interest for each sub-circuit.
- ③. Apply an appropriate signal to the large-scale circuit, simulate the accessible node voltages, and calculate the feature vectors.
- ④. For each sub-circuit, pass the feature vectors through

of sub-circuits can be summarized as:

- ①. Define the faults of interest for the circuit
- ②. Apply an appropriate signal to the circuit, measure the accessible node voltages, and calculate the feature vectors
- ③. Pass the feature vectors through BPNNs under various faults (including fault-free) conditions and train the BPNNs
- ④. Identify the faults at the output of the BPNN

BPNNs under various faults (including fault-free) conditions and train the BPNNs.

- ⑤. Apply the same signal to the large-scale circuit, measure the accessible node voltages, and classify these nodes into three classes.
- ⑥. Calculate the measured feature vectors of the sub-circuits which contain Class 3 and apply the feature vectors through the corresponding trained BPNNs.
- ⑦. Identify the faults from the output of the BPNNs.

4. ILLUSTRATIVE EXAMPLES

let us consider the circuit shown in Figure 3. The circuit is torn to 4 sub-networks. The accessible nodes are 3, 4, 7, 8, 12, 13, 14, 15, 17, 18, 21 and 22. The resistors and capacitors are assumed to have tolerances of 10%, and the transistors are modeled with the GP models in PSPICE, with 10% tolerance. The intervals of the accessible node voltages simulated are shown in Table 1. The circuit was measured three times for three different faults and the classes of the accessible nodes were determined. The measured voltages and the determined classes are also given in Table 1. The classes are the same for the three measurements. By the theorem, the faults must be in sub-circuit x_3 . Pass the feature vectors through the trained BPNN and the result of the BPNN shows that the faulty component is R_{14} . In fact, the faults were set to be R_{14} being short-circuited, open-circuited and of value of 450ohms, respectively. The diagnosis results are right, showing the validity of the technique.

5. CONCLUSIONS

A large-scale analogue circuit can be divided into several blocks/sub-networks using certain rules and the accessible (tearing) nodes can be classified into three classes. The components in Class 1 are fault free, and those in Class 2 are also fault free except the common branches of Classes 2 and 3. Therefore the fault components must be Class 3. This reduces the diagnosis problem of a large-scale circuit to locating the faults within the sub-circuits containing Class 3 only, thus reduced after-test computation and time. The neural network method is adopted to find faults at the component level, which make it possible to cope with tolerance effects, soft faults and on-line diagnosis. The nontrivial examples have confirmed the validity of the proposed technique.

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REFERENCES

- [1] J. W. Bandler and A. E. Salama, "Fault diagnosis of analog circuits," *Proceedings of IEEE*, Vol.73, No.8, pp.1279-1325, 1985.
- [2] R. W. Liu, ed., *Testing and Diagnosis of Analog Circuits and Systems*, Van Nostrand Reinhold, USA, 1991.
- [3] Y. Sun, "Class fault diagnosis theory and approaches", *Journal of China Institute of Communications*, Vol.11, No.5, 1990.
- [4] Y. Sun, "Investigation on diagnosis of the faulty branch-set class," *Journal of China Institute of Communications*, Vol.13, No.3, 1992.
- [5] Y. Sun and J. K. Fidler, "A topological method of class-fault diagnosis," *Proc. IEEE Midwest Symp. on Circuits and Systems*, Washington DC, USA, 1992.
- [6] R. Spain and S. Upadhyaya, "Linear circuit fault diagnosis using neuromorphic analyzers", *IEEE Trans. CAS-II*, Vol.44, No.3, pp.188-196, 1997.
- [7] T. Sorsa, H. N. Koivo, and H. Koivisto, "Neural networks in process fault diagnosis", *IEEE Trans. on Systems, Man and Cybernetics*, Vol.21, No.4, pp.815-825, 1991.
- [8] A. Bernieri, M.D'Apuzzo, L. Somson, etc, "A neural network approach for identification and fault diagnosis of dynamic systems", *IEEE Trans. IM*, Vol.43, No.6, 1994.
- [9] A. Srinivasan and C. Batur, "Hopfield/Art-1 neural network-based fault detection and fault diagnosis of dynamic systems", *IEEE Trans. Neural Networks*, Vol.5, No.6, pp.890-899, 1994.
- [10] Y. He and Y. Sun, "Neural networks-based L1-norm optimization approach for fault diagnosis of nonlinear circuits with tolerance," *IEE Proceedings: Circuits, Devices and Systems*, Vol. 148, No.4, pp.223-228, August 2001.
- [11] Y. He and Y. Sun, "Fault isolation in nonlinear analog circuits with tolerances using neural networks," *Proc. IEEE Int. Symp. Circuits and Systems*, pp.854-857, Sydney, 2001.
- [12] Y. He, Y. Ding and Y. Sun, "Fault diagnosis of analog circuits with tolerances using artificial neural networks," *Proc. IEEE APCCAS*, pp.292-295, Tianjin, China, 2000.
- [13] Y. He, Y. Tan and Y. Sun, "A neural network approach for fault diagnosis of large-scale analog circuits", *Proc. IEEE ISCAS*, pp.153-156, Arizona, USA, 2002.

Table1. The data of Figure 3

Node	simulated interval	test 1	class	test 2	class	test 3	class
3	[0.9114, 1.0731]	1.0716	1	0.9681	1	1.0584	1
4	[0.9114, 1.0731]	1.0717	1	0.9680	1	1.0585	1
7	[-0.8412, -0.8435]	-0.8406	1	-0.8434	1	-0.8409	1
8	[-2.7448, -2.7464]	-2.7763	1	-2.7250	1	-2.7696	1
12	[0.3230, 0.3235]	0.3779	2	0.2832	2	0.3658	2
13	[0.3230, 0.3235]	0.3779	2	0.2819	2	0.3670	2
14	[3.6248, 3.6289]	1.3710	3	5.0547	3	1.8844	3
15	[3.6248, 3.6289]	5.9656	3	2.1401	3	5.4309	3
17	[-.4103, -0.4131]	-0.0182	3	-0.4673	3	-0.3278	3
18	[0.5170, 0.5196]	-0.5867	2	-0.4673	2	-0.5715	2
21	[2.8852, 2.8868]	0.0072	2	4.3013	2	1.1688	2
22	[2.8852, 2.8868]	5.2067	2	1.4193	2	4.6755	2